REMARKS

The Examiner rejected claims 1, 2 and 4 under 35 USC 103(a) as being unpatentable over Ito (US 5,515,103) in view of Suzuki (US 4,686,571) and Watanabe (US 5,731,833). Applicants respectfully traverse this rejection.

Claims 1, 2 and 4 each require using two clock signals having different frequencies to drive a solid-state imaging apparatus. One clock signal is used for vertically transferring information charges from a light receiving portion to a storing portion, and the other clock signal is used to horizontally transfer the information charges from the storing portion to a horizontal transfer portion. The frequency of the clock signal used for vertical transferring is higher than that of the other clock signal used for horizontal transferring. This enables a quick transfer of the information charges from the light receiving portion to the storing portion, even if light receiving period is altered. Accordingly, the claimed invention can reduce smear components even when the exposure time of the imaging apparatus is increased.

Ito shows a timing control circuit 6 which receives a horizontal synchronizing signal H-SYC and a vertical synchronizing signal V-SYC. However, the synchronizing signals H-SYC and V-SYC are used to synchronize vertical transfer timing and horizontal transfer timing to each other. Therefore, Ito does not disclose using two clock signals to drive a solid-state imaging apparatus. Further, Ito does not suggest that one clock signal used for vertical transferring has a frequency higher than that of another clock signal used for horizontal transferring.

Suzuki discloses a method for driving a solid-state imaging apparatus using a clock signal. The frequency of the clock signal is switched between a first frequency and a second frequency. More specifically, in a light receiving operation, the clock signal having the first frequency is used. In a read-out operation, the clock signal having the second frequency is used. However, Suzuki does not disclose providing an image unit and a read-out register unit with two different clock signals, respectively. Further, Suzuki does not suggest that one clock signal used for vertical transferring has a frequency higher than that of another clock signal used for horizontal transferring.

Watanabe discloses generating a horizontal timing signal HT and a vertical timing signal VT from a constant reference clock CK. However, Watanabe does not suggest that the frequency of the vertical timing signal VT is higher than that of the horizontal timing signal HT.

None of the references suggest that one clock signal used for vertical transferring has a frequency higher than that of another clock signal used for horizontal transferring. Thus, claims 1, 2 and 4 are unobvious over Ito in view of Suzuki and Watanabe. Accordingly, Applicants respectfully request that the rejection be reconsidered and withdrawn, and that claims 1 – 5 be allowed.

The Examiner also rejected claims 1, 2 and 4 under 35 USC 103(a) over Applicants' admitted prior art in view of Suzuki. Applicants respectfully traverse this rejection.

Neither Applicants' admitted prior art nor Suzuki suggests that one clock signal used for vertical transferring has a frequency higher than that of another clock signal used for horizontal transferring. As the Examiner admitted, the Applicants' admitted prior art does not "disclose that the vertical drive circuit generates a vertical transfer clock from a second clock, which is shorter than the first clock, or that the horizontal transfer clock generates a horizontal transfer clock from the first clock." As discussed above, Suzuki also fails to disclose, teach or suggest providing an image unit and a read-out register unit with two different clock signals or that the clock signal used for vertical transferring has a frequency higher than that of the other clock signal used for horizontal transferring. Thus, claims 1, 2 and 4 are unobvious from Applicants' admitted prior art in view of Suzuki. Accordingly, Applicants respectfully request that the rejection be reconsidered and withdrawn and that claims 1-5 be allowed.

CONCLUSION

Claims 1 – 5 are pending in the application. The Examiner has rejected claims 1, 2 and 4 and objected to claims 3 and 5 as being allowable, but dependent upon rejected base claims. Applicants have respectfully traversed the rejection. Accordingly, Applicants believe the application to be in a condition for allowance. Applicants respectfully request that the rejections be reconsidered and withdrawn and that claims 1–5 be allowed. The Examiner is encouraged to contact the undersigned if it is believed that a telephone conference may expedite the prosecution of the application.

Respectfully submitted,

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